

PRELIMINARY

NCT5868D

PCIe to PCI Bridge

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1. GENERAL DESCRIPTION

The NCT5868D is a PCI Express to PCI Bridge that provides a solution to connect legacy PCI bus to PCI Express serial bus. The NCT5868D implements PCI Express as a primary bus and PCI as a second bus. With Bridge, existing PCI components can plug into PCI Express based system.

The NCT5868D is fully compliant with *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0 and supports a transparent forward bridge scheme. It support not only the standard PCI-to PCI bridge program model, but also the “Legacy mode” – support PCI-to-PCI bridge with subtractive decode.

The PCI Express port is fully compliant with PCI Express Base Specification, Revision 1.1. It supports an X1 link operation, allowing 250Mbps throughput in the upstream and downstream direction. It supports a Maximum Payload Size (MPS) of 128 bytes, AER & ECRC, single virtual channel, legacy power management and ASPM L0s.

The PCI port is 32 bits wide and operates at 33 MHz. It is fully compliant with *PCI Local Bus Specification*, Revision 3.0. The NCT5868D provides a built-in arbiter and PCI clock buffer supported 4 external PCI master. It supports fully VGA/ISA addressing for legacy operation.

The NCT5868D also contain a two wire signal bus to supports EEPROM initialization and internal register access and eight General Purpose I/O GPIO pins (GPIOs) for future system usage.

The NCT5868D can provide port80 code debugging support. It can output port80 code from the two wire signal bus or directly drive two 7-segment LEDs to display.

The NCT5868D can operate from a single 3.3v power supply, to reduce system cost.

PRELIMINARY**2. FEATURE****Bridge**

- PCI Express-to-PCI Bridge Specification 1.0
- PCI Express 1.1 X1 port
- PCI Local Bus Specification 3.0
- Forward bridge
- 8 GPIOs
- Single 3.3V power supply
- Support P2P bridge with subtractive decode

PCI Express Interface

- PCI Express Base Specification 1.1
- X1 at 2.5GHz
- PCI Express differential reference clock
- 128 Bytes payload
- Single virtual channel
- Error report and ECRC support
- Advanced Error Reporting(AER) support
- Supports up to 4KB data payload transfer
- Supports all Memory, I/O, Configuration, and Message transactions
- Native Active State Power Management L0s and L1 state support
- Power Management Event(PME message) and Beacon(Wake-Up) support
- MSI and INT message support
- MSI-X Capability Support

PCI interface

- PCI Local Bus Specifications 3.0
- 32-bit 33/66 MHz 5V tolerant IO
- Built-in arbiter support for 4 external masters
- Built-in PCI clock buffer for 4 external devices
- Support 4 legacy interrupts
- Provide three options for PCI 33/66MHz source
 - (1) from external 12MHz crystal
 - (2) from internal PCIe 100MHz
 - (3) from external 33/66MHZ

Power Management

- Legacy power management and ASPM L0s support
- PME# interrupts route to PCI Express
- Side-band WAKE_N signals

I2C support

- Optional EEPROM initialization for internal register access

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- Get Port80 message through I2C slave

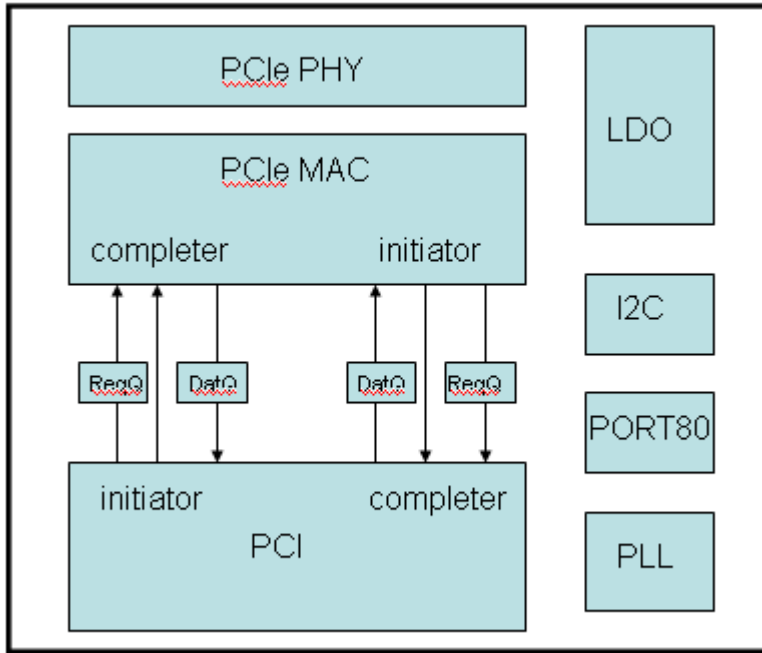
Port 80 Debugging support

- Decode IO space port 80/90/84.
- Direct drive 2 seven segment LEDs.

Package

- 128-pin LQFP
- Green/RoHS

3. FUNCTIONAL BLOCK



4. PIN LAYOUT

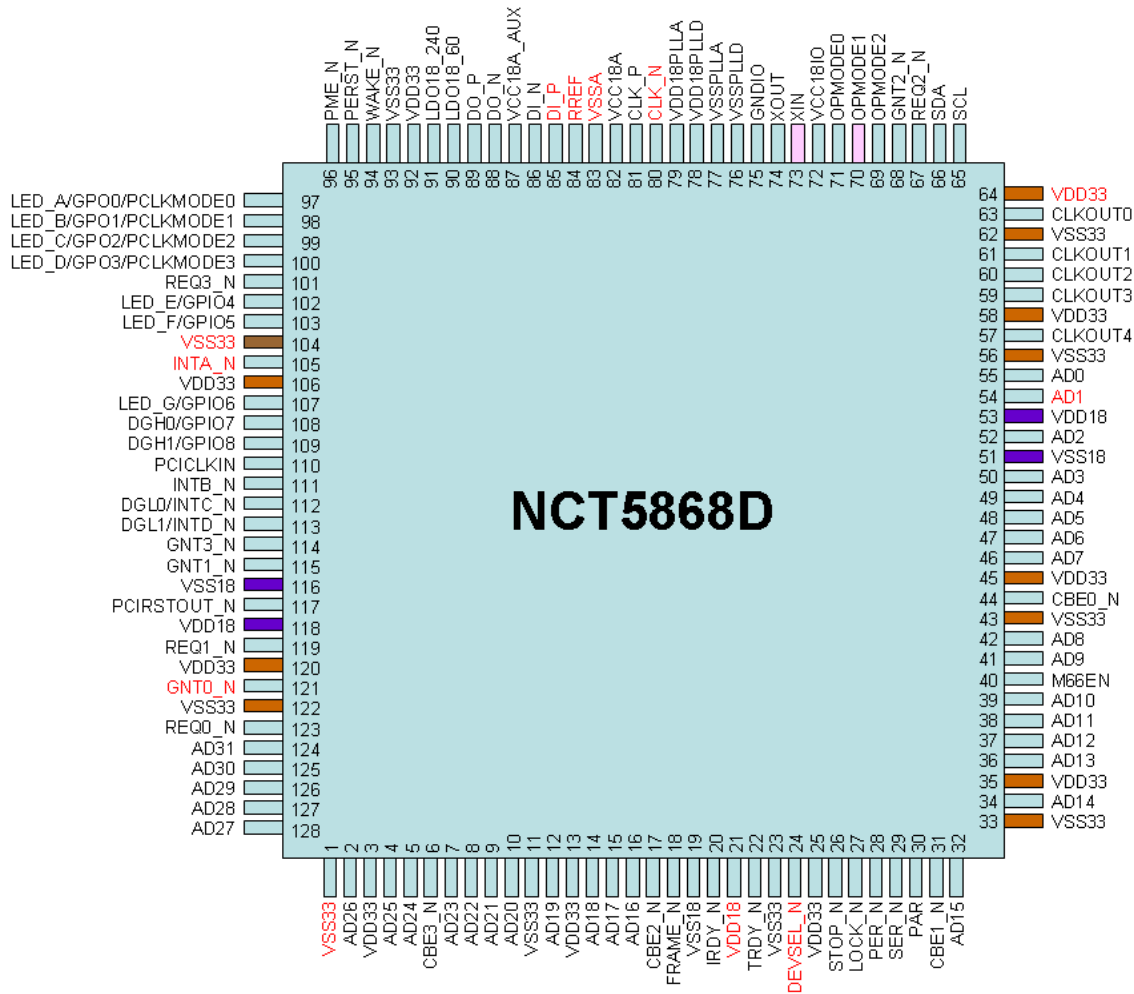


Figure 4-1 Pin Layout for NCT5868D

PRELIMINARY**5. PIN DESCRIPTION**

Note: DC/AC CHARACTERISTICS for details.

GNDIOD - Ground for 3.3V I/O
VCC3IOD - 3.3V power supply for digital IO
VCC18IO - 1.8V power supply for Crystal IO
GNDIO - Ground for Crystal IO
GNDKD - Ground for core logic cells
VCKD - Power supply for core logic cells
XPCIXD - PCI input buffer
YPCIH D - PCI output buffer
ZPCIAHD - PCI bi-direction buffer
UROSCHINTD - Crystal buffer

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5.1 PCI 32-bit Bus Interface Pin Assignments

Table 1: PCI 32-bit Bus Interface Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description
2	AD26	T/S I/O	ZPCIAHD	PCI Address/Data
4	AD25	T/S I/O	ZPCIAHD	PCI Address/Data
5	AD24	T/S I/O	ZPCIAHD	PCI Address/Data
6	CBE3_N	T/S I/O	ZPCIAHD	PCI Command/Byte Enable [3]
7	AD23	T/S I/O	ZPCIAHD	PCI Address/Data
8	AD22	T/S I/O	ZPCIAHD	PCI Address/Data
9	AD21	T/S I/O	ZPCIAHD	PCI Address/Data
10	AD20	T/S I/O	ZPCIAHD	PCI Address/Data
12	AD19	T/S I/O	ZPCIAHD	PCI Address/Data
14	AD18	T/S I/O	ZPCIAHD	PCI Address/Data
15	AD17	T/S I/O	ZPCIAHD	PCI Address/Data
16	AD16	T/S I/O	ZPCIAHD	PCI Address/Data
17	CBE2_N	T/S I/O	ZPCIAHD	PCI Command/Byte Enable [2]
18	FRAME_N	S/T/S I/O	ZPCIAHD	PCI Cycle Frame - Indicate the beginning of a PCI Transition
20	IRDY_N	S/T/S I/O	ZPCIAHD	PCI Initiator Ready - Assert by the transition initiator, indicate is ready for driving or accept data
22	TRDY_N	S/T/S I/O	ZPCIAHD	PCI Target Ready - Assert by the addressed target, indicate the target is ready to complete the current data cycle
24	DEVSEL_N	S/T/S I/O	ZPCIAHD	PCI Device Select - assert by a target when the target has decoded its address
26	STOP_N	S/T/S I/O	ZPCIAHD	The target assert STOP_N to indicate that it wishes the initiator to stop the transition
27	LOCK_N	S/T/S I/O	ZPCIAHD	Used by the initiator to lock the currently addressed memory target during an automic transition
28	PER_N	S/T/S I/O	ZPCIAHD	PCI data Parity Error
29	SER_N	O/D I/O	ZPCIAHD	PCI System Error

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30	PAR	T/S I/O	ZPCIAHD	PCI Parity - This is the even parity bit associated with the AD[31:0] and CBE_N[3:0]
31	CBE1_N	T/S I/O	ZPCIAHD	PCI Command/Byte Enable [1]
32	AD15	T/S I/O	ZPCIAHD	PCI Address/Data
34	AD14	T/S I/O	ZPCIAHD	PCI Address/Data
36	AD13	T/S I/O	ZPCIAHD	PCI Address/Data
37	AD12	T/S I/O	ZPCIAHD	PCI Address/Data
38	AD11	T/S I/O	ZPCIAHD	PCI Address/Data
39	AD10	T/S I/O	ZPCIAHD	PCI Address/Data
40	M66EN	I	XPCIXD	PCI 66MHz enable
41	AD9	T/S I/O	ZPCIAHD	PCI Address/Data
42	AD8	T/S I/O	ZPCIAHD	PCI Address/Data
44	CBE0_N	T/S I/O	ZPCIAHD	PCI Command/Byte Enable [0]
46	AD7	T/S I/O	ZPCIAHD	PCI Address/Data
47	AD6	T/S I/O	ZPCIAHD	PCI Address/Data
48	AD5	T/S I/O	ZPCIAHD	PCI Address/Data
49	AD4	T/S I/O	ZPCIAHD	PCI Address/Data
50	AD3	T/S I/O	ZPCIAHD	PCI Address/Data
52	AD2	T/S I/O	ZPCIAHD	PCI Address/Data
54	AD1	T/S I/O	ZPCIAHD	PCI Address/Data
55	AD0	T/S I/O	ZPCIAHD	PCI Address/Data
57	CLKOUT4	O	YPCIHD	PCI Clock Output [4]
59	CLKOUT3	O	YPCIHD	PCI Clock Output [3]
60	CLKOUT2	O	YPCIHD	PCI Clock Output [2]
61	CLKOUT1	O	YPCIHD	PCI Clock Output [1]
63	CLKOUT0	O	YPCIHD	PCI Clock Output [0]
67	REQ2_N	I	XPCIXD	PCI Bus Request [2]
68	GNT2_N	O	YPCIHD	PCI Bus Grant [2]
96	PME_N	I	XPCIXD	PCI Power Management Event

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101	REQ3_N	I	XPCIXD	PCI Bus Request [3]
105	INTA_N	I	XPCIXD	PCI Interrupt Request A
110	PCICLKIN	I	XPCIXD	PCI clock input
111	INTB_N	I	XPCIXD	PCI Interrupt Request B
112	DGL0/INTC_N	T/S I/O	XPCIXD	PCI Interrupt Request C 7-Segment LED common pin
113	DGL1/INTD_N	T/S I/O	XPCIXD	PCI Interrupt Request D 7-Segmenr LED common pin
114	GNT3_N	O	YPCIHD	PCI Bus Grant [3]
115	GNT1_N	O	YPCIHD	PCI Bus Grant [1]
119	REQ1_N	I	XPCIXD	PCI Bus Request [1]
121	GNT0_N	O	YPCIHD	PCI Bus Grant [0]
123	REQ0_N	I	XPCIXD	PCI Bus Request [0]
124	AD31	T/S I/O	ZPCIAHD	PCI Address/Data
125	AD30	T/S I/O	ZPCIAHD	PCI Address/Data
126	AD29	T/S I/O	ZPCIAHD	PCI Address/Data
127	AD28	T/S I/O	ZPCIAHD	PCI Address/Data
128	AD27	T/S I/O	ZPCIAHD	PCI Address/Data

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5.2 PCI Express Interface Pin Assignments

Table 2: PCI Express Interface Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description
80	CLK_N	I	PCIe PHY	PCIe differential negative clk
81	CLK_P	I		PCIe differential positive clk
82	VCC18A	I		PCIe PHY analog power
83	VSSA	I		PCIe PHY analog ground
84	RREF	O		12K Ohm resistor for Reference current
85	DI_P	I		PCIe differential positive input
86	DI_N	I		PCIe differential negative input
87	VCC18A_AUX	I		PCIe analog power
88	DO_N	O		PCIe differential negative output
89	DO_P	O		PCIe differential positive output
94	WAKE_N	OD		YPCIHD

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5.3 Reset Pin Assignments

Table 3: Reset Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description
95	PERST_N	I	XPCIXD	Reset In
117	PCIRSTOUT_N	O	YPCIHD	Reset Out

5.4 Miscellaneous Pin Assignments

Table 4: Miscellaneous Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description	
65	SCL	O/D I/O	ZPCIAHD	mode: 000 I2C master mode SCL mode: 001 I2C slave mode SCL mode: 1xx test mode	
66	SDA	O/D I/O	ZPCIAHD	mode: 000 I2C master mode SDA mode: 001 I2C slave mode SDA mode: 1xx test mode	
69	OPMODE2	I	XPCIXD	OPMODE[2:0] 000: Normal mode with GPIO, EEPROM loader 001: Normal mode with GPIO, I2C slave 010: Normal mode with 7-segment, EEPROM loader 011: Normal mode with 7-segment, I2C slave 1xx : reserved	
70	OPMODE1	I	XPCIXD		
71	OPMODE0	I	XPCIXD		
97	LED_A/GPO0/ PCLKMODE0	T/S O	ZPCIAHD		
98	LED_B/GPO1/ PCLKMODE1	T/S O	ZPCIAHD	GPO[1] 7-Segment LED_B	
99	LED_C/GPO2/ PCLKMODE2	T/S O	ZPCIAHD	GPO[2] 7-Segment LED_C	
100	LED_D/GPO3/ PCLKMODE3	T/S O	ZPCIAHD	GPO[3] 7-Segment LED_D	
102	LED_E/GPIO4	T/S I/O	ZPCIAHD	GPIO[4] 7-Segment LED_E	
103	LED_F/GPIO5	T/S I/O	ZPCIAHD	GPIO[5] 7-Segment LED_F	
107	LED_G/GPIO6	T/S I/O	ZPCIAHD	GPIO[6] 7-Segment LED_G	
108	DGH0/GPIO7	T/S I/O	ZPCIAHD	GPIO[7] 7-Segment LED common pin	
109	DGH1/GPIO8	T/S I/O	ZPCIAHD	GPIO[8] 7-Segment LED common pin	

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5.5 Analog Interface Pin Assignments

Table 5: Analog Interface Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description
73	XIN	I	UROSCHINTD	12MHz xtal in
74	XOUT	O	UROSCHINTD	12MHz xtal out

5.6 Power/Ground Interface Pin Assignments

Table 6: Power/Ground Interface Pin Assignments

Pin	Pin Name	Type	IO Buffer	Pin Description
1	VSS33	G	GNDIOD	Ground for 3.3V I/O
3	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
11	VSS33	G	GNDIOD	Ground for 3.3V I/O
13	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
19	VSS18	G	GNDKD	Ground for core logical cells
21	VDD18	P	VCCKD	Power for core logical cells Connect this pin to decupling capacitor
23	VSS33	G	GNDIOD	Ground for 3.3V I/O
25	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
33	VSS33	G	GNDIOD	Ground for 3.3V I/O
35	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
43	VSS33	G	GNDIOD	Ground for 3.3V I/O
45	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
51	VSS18	G	GNDKD	Ground for core logical cells
53	VDD18	P	VCCKD	Power for core logical cells Connect this pin to decupling capacitor
56	VSS33	G	GNDIOD	Ground for 3.3V I/O
58	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
62	VSS33	G	GNDIOD	Ground for 3.3V I/O
64	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
72	VCC18IO	P	VCC18IO	1.8V Crystal PAD power
75	GNDIO	G	GNDIO	Ground for Crystal PAD
76	VSSPLL	G	PLL PAD	PLL digital ground
77	VSSPLLA	G		PLL analog ground
78	VDD18PLL	P		PLL digital power
79	VDD18PLLA	P		PLL analog power

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90	LDO18_60		LDO PAD	1.8V output with 60mA
91	LDO18_240			1.8V output with 240mA
92	VDD33	P		3.3V powersupply
93	VSS33	G		LDO ground
104	VSS33	G	GNDIOD	Ground for 3.3V I/O
106	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
116	VSS18	G	GNDKD	Ground for core logical cells
118	VDD18	P	VCCKD	Power for core logical cells Connect this pin to decupling capacitor
120	VDD33	P	VCC3IOD	3.3V power supply for digital I/O
122	VSS33	G	GNDIOD	Ground for 3.3V I/O

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6. SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	-0.3 to +3.6	V
Input Voltage	-0.3 to +3.6	V
Operating Voltage	0 to +70	°C
Storage Temperature	-55 to +150	°C

6.2 DC/AC CHARACTERISTICS

($T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Power supply for core logic cells	VCKKD	1.62		1.98	V	
3.3V power supply for digital IO	VCC3IOD	3.0		3.6	V	
Input High Voltage	Vih	$0.5 \cdot V_{CC3IOD}$		$V_{CC3IOD} + 0.5$	V	
Input Low Voltage	Vil	-0.5		$0.3 \cdot V_{CC3IOD}$	V	
Output High Voltage	Voh	$0.9 \cdot V_{CC3IOD}$			V	$I_{out} = 500\mu\text{A}$
Output Low Voltage	Vol			$0.1 \cdot V_{CC3IOD}$	V	$I_{out} = 1500\mu\text{A}$
PCI-66						
Switching Current High	$I_{oh}(AC)$			$-32 \cdot V_{CC3IOD}$	mA	$V_{out} = 0.7 \cdot V_{CC3IOD}$
Switching Current Low	$I_{oh}(AC)$	$-12 \cdot V_{CC3IOD}$			mA	$V_{out} = 0.3 \cdot V_{CC3IOD}$
Switching Current Low	$I_{ol}(AC)$			$38 \cdot V_{CC3IOD}$	mA	$V_{out} = 0.18 \cdot V_{CC3IOD}$
Switching Current Low	$I_{ol}(AC)$	$16 \cdot V_{CC3IOD}$			mA	$V_{out} = 0.6 \cdot V_{CC3IOD}$
PCI-33						
Switching Current High	$I_{oh}(AC)$	$-12 \cdot V_{CC3IOD}$			mA	$0 < V_{out} \leq 0.3 \cdot V_{CC3IOD}$
Switching Current High	$I_{oh}(AC)$	$-17.1 \cdot (V_{CC3IOD} - V_{out})$			mA	$0.3 \cdot V_{CC3IOD} < V_{out} < 0.9 \cdot V_{CC3IOD}$

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PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Switching Current High	I _{oh} (AC)			Eq't'n C*	mA	0.7*VCC3IOD <Vout<VCC3IOD
Switching Current Low	I _{ol} (AC)	16*VCC3IOD			mA	0.6*VCC3IOD <=Vout<VCC3IOD
Switching Current Low	I _{ol} (AC)	26.7*Vout			mA	0.1*VCC3IOD <Vout<0.6*VCC3IOD
Switching Current Low	I _{ol} (AC)			Eq't'n D**	mA	0<Vout<0.18*VCC3IOD

Eq't'n C: I_{oh}=(98.0/VCC3IOD)(Vout-VCC3IOD)*(Vout+0.4VCC3IOD) for 0.7*VCC3IOD<Vout<VCC3IOD

** Eq't'n D: I_{ol}=(256/VCC3IOD)*Vout*(VCC3IOD-Vout) for 0<Vout<0.18*VCC3IOD

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7. FEATURE DESCRIPTION

7.1 Legacy mode support

Legacy mode requires special requirements from chipset and BIOS. In this mode both the root port and PCIe-to-PCI Bridge are configured to look like subtractive PCI-to-PCI bridges. The goal is to make this look like a PCI hierarchy to the OS, and has legacy address support.

When configured as a subtractive bridge, both the PCH PCIe root port and the PCIe-to-PCI Bridge will positively forward downstream transactions that fall within their bridge base and limit registers and will subtractively forward all downstream transactions that do not positively target any other functions.

If user is going to use legacy mode, BIOS need to setup chipset and NCT5868D to enable subtractive decode capability. About detail scheme for chipset setup, please check with chipset vendor (Intel). For bridge setup, NCT5868D provide **Legacy Mode Enable** (Register Offset 04h, Bit 11). Its default value is 0(disable). When BIOS program it to 1(enable), then NCT5868D will enable legacy mode and OS will treat it as subtractive PCI-to-PCI bridges if chipset is also setup.

7.2 PCI 33/66MHz source selection

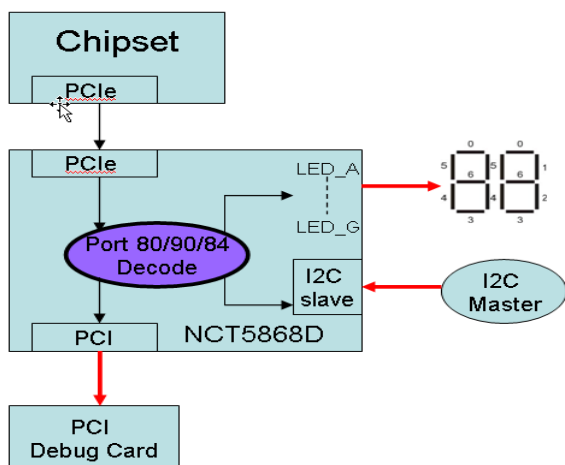
NCT5868D provide three kinds of PCI 33/66 clock source selection – from external crystal, from PCIe 100MHz or from external 33/66MHz. User can use 4 strapping pin PCLKMODE[3:0](pin97~pin100) to decide which clock source will be chosen when system booting. Below is strapping selection list.

PCI 33/66 clock source	PCLK MODE0	PCLK MODE1	PCLK MODE2	PCLK MODE3
External 12MHz crystal => PCI 33MHz	0	0	0	0
Internal PCIe 100MHz => PCI 33MHz	1	0	0	0
External 12MHz crystal => PCI 66MHz	0	1	0	0
Internal PCIe 100MHz => PCI 66MHz	1	1	0	0
External 33/66MHz => PCI 33/66MHz from	0	0	1	0

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7.3 Port 80/90/84 Message decode

NCT5868D can decode port80/90/84 debug message from PCIe root port if BIOS enable legacy mode on both chipset & bridge. NCT5868D provide **PORT DECODE SELECTION** (Register Offset CEh, Bit 0). Its default value is 0(port80 and 90 message are decoded together). When BIOS program it to 1, NCT5868D will decode port84 message only. There are three ways to output specific port message and listed as below:



7.3.1 Output through 7-segment LEDs

NCT5868D provide 7-segment LED interface and can drive two common cathode 7-segment LEDs directly to output port 80/90/84 message. When **OPMODE[2:0]** (pin71,70,69) hardwire to **010** or **011**, NCT5868D will output specific port message to on-board 7-segments.

7.3.2 Output through I2C slave

NCT5868D provide I2C slave interface to output specific port message. User can use external I2C master to read NCT5868D I2C slave address 08h and minimum speed is 100KHz. When **OPMODE[2:0]** (pin71,70,69) hardwire to **001** or **011**, NCT5868D will enable this message output path

7.3.3 Output through PCI bus

User still can use traditional port80 debug card to get port80 message from PCI bus as long as BIOS enable legacy mode on both chipset & bridge without any other register configuration.

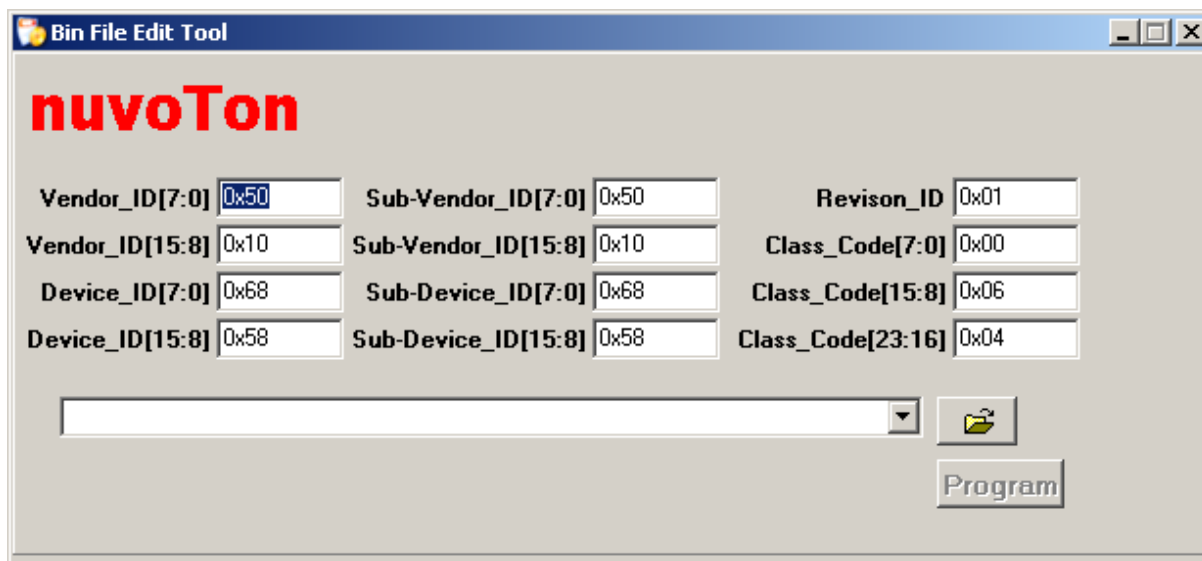
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7.4 I2C EEPROM initialization

NCT5868D provides EEPROM boot loader function. User can modify some below register default value through EEPROM when booting.

Register Offset	Register location	Register Description
0x00	15:0	Vendor ID
0x02	15:0	Device ID
0x08	15:0	Revision ID
0x09	15:0	Class Code
0xC4	7:0	Subsystem Vendor ID
0xC6	23:0	Subsystem Device ID

Nuvoton provides a “EEPROM Bin Editor” for user to generate bin file according to user’s specific value. If you need this kind of support, please contact with Nuvoton.



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7.5 OPMODE Selection

Because NCT5868D integrate GPIO and 7-segments LED on multi-function pins, I2C slave and EEPROM boot loader on multi-function pins, NCT5868D use OPMODE2(pin69), OPMODE1(pin70) and OPMODE0(pin71) as strapping pin. Below is strapping selection list:

Function operation	OPMODE2	OPMODE1	OPMODE0
GPIO & EEPROM Loader	0	0	0
GPIO & I2C Slave	0	0	1
7-Segments & EEPROM Loader	0	1	0
7-Segment & I2C Slave	0	1	1
Reserved	1	x	x

7.6 Support for subsystem ID(SSID) and Subsystem vendor ID(SSVID)

From 7.4, user can modify some register default value through external EEPROM when booting, including SSID and SSVID. But user also can modify SSID and SVID through another backdoor scheme.

NCT5868D provide **SSID SSVID Enable** (Register Offset CFh, Bit 0). Its default value is 0 and when user sets it to 1, **SSID** (Register Offset C4h, Bit[7:0]) and **SSVID** (Register Offset C6h, Bit[23:0]) will become from “Read-only” to “Read-Write”. User can fill the expect value to **SSID & SSVID**, then change back **SSID SSVID Enable** to 0. The SSID and SSVID will recovery to original Read-only type and keep new default value.

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8. BRIDGE REGISTER

8.1 Type 0 Configuration Settings

31:24	23:16	15:8	7:0	Byte Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header Type	Latency Timer	Cache Line Size	00Ch
Base Address 0				010h
Base Address 1				014h
Base Address 2				018h
Base Address 3				01Ch
Base Address 4				020h
Base Address 5				024h
				028h
Subsystem ID		Subsystem Vendor ID		02Ch
Expansion ROM base address				030h
			Capabilities PTR	034h
				038h
Max_Lat	Min_Gnt	Int. Pin	Int. Line	03Ch

8.1.1 Register Offset 000h – Vendor ID

Bit(s)	Description	CFG	Default
15:0	Vendor ID Identifies the manufacturer.	RO	1050h

8.1.2 Register Offset 002h – Device ID

Bit(s)	Description	CFG	Default
15:0	Device ID Identifies the particular device, as specified by the vendor.	RO	5868h

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8.1.3 Register Offset 004h – Command Register

Bit(s)	Description	CFG	Default
0	I/O Access Enable Enables I/O Space accesses on the primary bus.	RW	0
1	Memory Space Enable Enables Memory Space accesses on the primary bus.	RW	0
2	Bus Master Enable Enables Memory and I/O Read/Write requests on the primary bus.	RW	0
3	Special Cycle Enable Does not apply to PCI Express; therefore, forced to 0.	RO	0
4	Memory Write and Invalidate 0 = Enables PCI Master logic to use the Memory Write command. 1 = Enables the PCI Master logic to use the Memory Write and Invalidate command.	RW	0
5	VGA Palette Snoop Does not apply to PCI Express; therefore, forced to 0.	RO	0
6	Parity Error Response Enable Controls the Data Parity errors forwarded from the primary bus. 0 = must ignore 1 = must take its standard action when a Data Parity error is detected.	RW	0
7	IDSEL Stepping/Wait Cycle Control Does not apply to PCI Express. Must be hardwired to 0	RW	0
8	SERR# Enable Enables reporting of Fatal and Non-Fatal errors to the Root Complex.	RW	0
9	Fast Back-to-Back Enable Does not apply to PCI Express; therefore, forced to 0.	RO	0
10	Interrupt Disable 1 = Controls the ability of a PCI Express device to generate INTx# Interrupt messages. When set, devices are prevented from generating INTx interrupt Messages. Any INTx emulation interrupts already asserted by the device must be deasserted when this bit is set.	RW	0
11	Legacy Mode Enable 1 = Enables Legacy Mode.	RW	0
15:12	Reserved		0

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8.1.4 Register Offset 006h – Status Register

Bit(s)	Description	CFG	Default
2:0	Reserved		0
3	Interrupt Status 1 = Indicates that an INTx# Interrupt message is pending on behalf of functions integrated into the Bridge. Does not reflect the status of INTx# inputs associated with the secondary bus.	RO	0
4	Capabilities List Indicates whether the Capabilities Pointer at offset 34h is valid. Because all PCI Express devices are required to implement the PCI Express Capability structure, this bit is hardwired to 1.	RO	1
5	66 MHz Capable Does not apply to PCI Express; therefore, forced to 0.	RO	0
6	Reserved		0
7	Fast Back-to-Back Transactions Capable Does not apply to PCI Express; therefore, forced to 0.	RO	0
8	Master Data Parity Error Used to report Data Parity error detection by the Bridge. Set when the Command register <i>Parity Error Response Enable</i> bit is set and either of the following two conditions occur: <ul style="list-style-type: none"> • Bridge receives a Completion marked poisoned on the primary bus • Bridge poisons a Write request or Read Completion on the primary bus Writing 1 clears this bit.	RW1C	0
10:9	DEVSEL Timing Does not apply to PCI Express; therefore, forced to 0.	RO	0
11	Signaled Target Abort Set when the Bridge completes a Request as a transaction Target on its primary bus, using Completer Abort Completion status. Writing 1 clears this bit.	RW1C	0
12	Received Target Abort Set when the Bridge receives a Completion with Completer Abort Completion status on its primary bus. Writing 1 clears this bit.	RW1C	0
13	Received Master Abort Set when the Bridge receives a Completion with Unsupported Request Completion status on its primary bus. Writing 1 clears this bit.	RW1C	0

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14	<p>Signaled System Error Set when the Bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the Command register <i>SERR# Enable</i> bit is set.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
15	<p>Detected Parity Error Set when the Bridge receives a poisoned TLP on the primary bus, regardless of the Command register <i>Parity Error Response Enable</i> bit state.</p> <p>Writing 1 clears this bit.</p>	RW1C	0

8.1.5 Register Offset 008h – Revision ID Register

Bit(s)	Description	CFG	Default
7:0	<p>Revision ID Identifies the Bridge Revision</p>	RO	01h

8.1.6 Register Offset 009h – Class Code Register

Bit(s)	Description	CFG	Default
7:0	Programming Interface	RO	00h
15:8	Sub-Class Code	RO	04h
23:16	Base Class Code	RO	06h

8.1.7 Register Offset 00Ch -- Cache Line Size Register

Bit(s)	Description	CFG	Default
7:0	<p>Cache Line Size Specifies the System Cache Line Size (in units of DWORDs). The value in this register is used to determine whether to use Read, Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands for accessing memory. 0h = 0 DWORDs 2h = 2 DWORDs 4h = 4 DWORDs 8h = 8 DWORDs 10h = 16 DWORDs 20h = 32 DWORDs</p> <p>Writes of values other than these result in a Cache Line Size of 0; however, the value written is returned when this register is read.</p>	RW	00h

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8.1.8 Register Offset 00Dh -- Master Latency Timer Register

Bit(s)	Description	CFG	Default
7:0	Master Latency Timer The Primary/Master Latency Timer does not apply to PCI Express.	RO	00h

8.1.9 Register Offset 00Eh -- Header Type Register

Bit(s)	Description	CFG	Default
7:0	Header Type bridges, this field is forced to 1h.	RO	01h

8.1.10 Register Offset 00Fh -- Built-In Self-Test Register

Bit(s)	Description	CFG	Default
7:0	Built-In Self-Test <i>Not supported</i> Always returns a value of 0h.	RO	00h

8.1.11 Register Offset 010h -- Base Address 0 (BAR0) Register

Bit(s)	Description	CFG	Default
0	Space Type When Low, this space is accessed as memory. When High, this space is accessed as I/O. <i>Note: Hardwired to 0.</i>	RO	0
2:1	Address Type Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = <i>Reserved</i>	RO	10b
3	Prefetch Enable 1 = Indicates that prefetching has no side effects on Reads	RO	1
15:4	Base Address This section of the Base address is ignored for a 64-KB space. <i>Note: Hardwired to 0.</i>	RO	0h
31:16	Base Address Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the Bridge Configuration registers and shared memory.	RW	0h

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8.1.12 Register Offset 014h -- Base Address 1 (BAR1) Register

Bit(s)	Description	CFG	Default
31:0	Base Address 1 Determines the upper 32 bits of the address when Base Address 0 is configured for 64-bit addressing.	RW	00h

8.1.13 Register Offset 018h -- Base Address 2 (BAR2) Register

8.1.14 Register Offset 01Ch -- Base Address 3 (BAR3) Register

8.1.15 Register Offset 020h -- Base Address 4 (BAR4) Register

8.1.16 Register Offset 024h -- Base Address 5 (BAR5) Register

8.1.17 Register Offset 02Ch -- Subsystem Vendor ID Register

Bit(s)	Description	CFG	Default
15:0	Subsystem Vendor ID Identifies the card manufacturer.	RO	1050h

8.1.18 Register Offset 02Eh -- Subsystem ID Register

Bit(s)	Description	CFG	Default
15:0	Subsystem ID Identifies the particular device, as specified by the subsystem vendor.	RO	5868h

8.1.19 Register Offset 030h -- Expansion ROM base address Register

Bit(s)	Description	CFG	Default
0	Expansion ROM base address Address Decode Enable. 1= indicates the device accepts accesses to the expansion ROM address. 0= indicates the device does not accept accesses to expansion ROM space. Should be set to 0 if no Expansion ROM.	RW	0
10:1	Reserved		0
31:11	Expansion ROM Base Address (upper 21 bits)	RW	0

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8.1.20 Register Offset 034h -- Capabilities Pointer Register

Bit(s)	Description	CFG	Default
7:0	PCI Capabilities Pointer Provides the offset location of the first New Capabilities register	RO	40h

8.1.21 Register Offset 03Ch -- Interrupt Line Register

Bit(s)	Description	CFG	Default
7:0	PCI Interrupt Line Interrupt Line Routing Value. Value indicates which input of the system interrupt controller(s) the Bridge interrupt line is connected to.	RW	0h

8.1.22 Register Offset 03Dh -- Interrupt Pin Register

Bit(s)	Description	CFG	Default
7:0	PCI Interrupt Pin Identifies the Conventional PCI Interrupt message(s) used by the Bridge. Valid values are 1, 2, 3, and 4, which map to Conventional PCI Interrupt messages for INTA# , INTB# , INTC# , and INTD# , respectively. 0h = Indicates that the Bridge does not use Conventional PCI Interrupt messages 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	RO	1h

8.1.23 Register Offset 03Eh -- Min_Gnt Register

Bit(s)	Description	CFG	Default
7:0	Min_Gnt. Used to specify how long a burst period the device needs assuming a clock rate of 33 MHz.	RO	0h

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8.1.24 Register Offset 03Fh -- Max_Lat Register

Bit(s)	Description	CFG	Default
7:0	Max_Lat. Used to specify how often the device needs to gain access to the PCI bus.	RO	0h

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8.2 Type 1 Configuration Settings

31:24	23:16	15:8	7:0	Byte Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
			Cache Line	00Ch
Base Address 0				010h
Base Address 1				014h
Sec Bus Latency	Sub Bus Number	Sec Bus Number	Prim Bus Number	018h
Secondary Status		I/O Limit	I/O Base	01Ch
Memory Limit		Memory Base		020h
Prefetchable Memory Limit		Prefetchable Memory Base		024h
Prefetchable Base Upper 32-bits				028h
Prefetchable Limit Upper 32-bits				02Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		030h
			Capabilities PTR	034h
Expansion ROM base address				038h
Bridge Control		Int. Pin	Int. Line	03Ch

8.2.1 Register Offset 000h – Vendor ID

Bit(s)	Description	CFG	Default
15:0	Vendor ID Identifies the manufacturer.	RO	1050h

8.2.2 Register Offset 002h – Device ID

Bit(s)	Description	CFG	Default
15:0	Device ID Identifies the particular device, as specified by the vendor.	RO	5868h

8.2.3 Register Offset 004h – Command Register

Bit(s)	Description	CFG	Default
0	I/O Access Enable Enables I/O Space accesses on the primary bus.	RW	0
1	Memory Space Enable Enables Memory Space accesses on the primary bus.	RW	0

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2	Bus Master Enable Enables Memory and I/O Read/Write requests on the primary bus.	RW	0
3	Special Cycle Enable Does not apply to PCI Express; therefore, forced to 0.	RO	0
4	Memory Write and Invalidate 0 = Enables PCI Master logic to use the Memory Write command. 1 = Enables the PCI Master logic to use the Memory Write and Invalidate command.	RW	0
5	VGA Palette Snoop Does not apply to PCI Express; therefore, forced to 0.	RO	0
6	Parity Error Response Enable Controls the Data Parity errors forwarded from the primary bus. 0 = must ignore 1 = must take its standard action when a Data Parity error is detected.	RW	0
7	IDSEL Stepping/Wait Cycle Control Does not apply to PCI Express. Must be hardwired to 0	RW	0
8	SERR# Enable Enables reporting of Fatal and Non-Fatal errors to the Root Complex.	RW	0
9	Fast Back-to-Back Enable Does not apply to PCI Express; therefore, forced to 0.	RO	0
10	Interrupt Disable 1 = Controls the ability of a PCI Express device to generate INTx# Interrupt messages. When set, devices are prevented from generating INTx interrupt Messages. Any INTx emulation interrupts already asserted by the device must be deasserted when this bit is set.	RW	0
15:11	Reserved		0

8.2.4 Register Offset 006h – Status Register

Bit(s)	Description	CFG	Default
2:0	Reserved		0
3	Interrupt Status 1 = Indicates that an INTx# Interrupt message is pending on behalf of functions integrated into the Bridge. Does not reflect the status of INTx# inputs associated with the secondary bus.	RO	0
4	Capabilities List Indicates whether the Capabilities Pointer at offset 34h is valid. Because all PCI Express devices are required to implement the PCI Express Capability structure, this bit is hardwired to 1.	RO	1

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5	66 MHz Capable Does not apply to PCI Express; therefore, forced to 0.	RO	0
6	Reserved		0
7	Fast Back-to-Back Transactions Capable Does not apply to PCI Express; therefore, forced to 0.	RO	0
8	Master Data Parity Error Used to report Data Parity error detection by the Bridge. Set when the Command register <i>Parity Error Response Enable</i> bit is set and either of the following two conditions occur: <ul style="list-style-type: none"> • Bridge receives a Completion marked poisoned on the primary bus • Bridge poisons a Write request or Read Completion on the primary bus Writing 1 clears this bit.	RW1C	0
10:9	DEVSEL Timing Does not apply to PCI Express; therefore, forced to 0.	RO	0
11	Signaled Target Abort Set when the Bridge completes a Request as a transaction Target on its primary bus, using Completer Abort Completion status. Writing 1 clears this bit.	RW1C	0
12	Received Target Abort Set when the Bridge receives a Completion with Completer Abort Completion status on its primary bus. Writing 1 clears this bit.	RW1C	0
13	Received Master Abort Set when the Bridge receives a Completion with Unsupported Request Completion status on its primary bus. Writing 1 clears this bit.	RW1C	0
14	Signaled System Error Set when the Bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the Command register <i>SERR# Enable</i> bit is set. Writing 1 clears this bit.	RW1C	0
15	Detected Parity Error Set when the Bridge receives a poisoned TLP on the primary bus, regardless of the Command register <i>Parity Error Response Enable</i> bit state. Writing 1 clears this bi	RW1C	0

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8.2.5 Register Offset 008h – Revision ID Register

Bit(s)	Description	CFG	Default
7:0	Revision ID Identifies the Bridge Revision	RO	01h

8.2.6 Register Offset 009h – Class Code Register

Bit(s)	Description	CFG	Default
7:0	Programming Interface	RO	00h
15:8	Sub-Class Code	RO	04h
23:16	Base Class Code	RO	06h

8.2.7 Register Offset 00Ch -- Cache Line Size Register

Bit(s)	Description	CFG	Default
7:0	Cache Line Size Specifies the System Cache Line Size (in units of DWORDs). The value in this register is used to determine whether to use Read, Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands for accessing memory. 0h = 0 DWords 2h = 2 DWords 4h = 4 DWords 8h = 8 DWords 10h = 16 DWords 20h = 32 DWords Writes of values other than these result in a Cache Line Size of 0; however, the value written is returned when this register is read.	RW	00h

8.2.8 Register Offset 00Dh -- Master Latency Timer Register

Bit(s)	Description	CFG	Default
7:0	Master Latency Timer The Primary/Master Latency Timer does not apply to PCI Express.	RO	00h

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8.2.9 Register Offset 00Eh -- Header Type Register

Bit(s)	Description	CFG	Default
7:0	Header Type bridges, this field is forced to 1h.	RO	01h

8.2.10 Register Offset 00Fh -- Built-In Self-Test Register

Bit(s)	Description	CFG	Default
7:0	Built-In Self-Test <i>Not supported</i> Always returns a value of 0h.	RO	00h

8.2.11 Register Offset 010h -- Base Address 0 (BAR0) Register

Bit(s)	Description	CFG	Default
0	Space Type When Low, this space is accessed as memory. When High, this space is accessed as I/O. <i>Note: Hardwired to 0.</i>	RO	0
2:1	Address Type Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = <i>Reserved</i>	RO	10b
3	Prefetch Enable 1 = Indicates that prefetching has no side effects on Reads	RO	1
15:4	Base Address This section of the Base address is ignored for a 64-KB space. <i>Note: Hardwired to 0.</i>	RO	0h
31:16	Base Address Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the Bridge Configuration registers and shared memory.	RW	0h

8.2.12 Register Offset 014h -- Base Address 1 (BAR1) Register

Bit(s)	Description	CFG	Default
31:0	Base Address 1 Determines the upper 32 bits of the address when Base Address 0 is configured for 64-bit addressing.	RW	00h

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8.2.13 Register Offset 018h -- Primary Bus Number Register

Bit(s)	Description	CFG	Default
7:0	Primary Bus Number Used to record the Bus Number of the PCI Bus segment to which the Bridge's primary bus is connected.	RW	00h

8.2.14 Register Offset 019h -- Secondary Bus Number Register

Bit(s)	Description	CFG	Default
7:0	Secondary Bus Number Used to record the Bus Number of the PCI Bus segment to which the Bridge's secondary bus is connected.	RW	00h

8.2.15 Register Offset 01Ah -- Subordinate Bus Number Register

Bit(s)	Description	CFG	Default
7:0	Subordinate Bus Number Used to record the Bus Number of the highest-numbered PCI Bus segment behind (or subordinate to) the Bridge.	RW	00h

8.2.16 Register Offset 01Bh -- Secondary Latency Timer Register

Bit(s)	Description	CFG	Default
7:0	Secondary Latency Timer Specifies (in PCI clock units) the Latency Timer value during secondary bus (PCI) Master bursts.	RW	00h

8.2.17 Register Offset 01Ch -- I/O Base Register

Bit(s)	Description	CFG	Default
3:0	I/O Base Address Capability Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are <i>reserved</i> .	RO	0h
7:4	I/O Base Determines the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the Bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are 000h.	RW	0h

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	Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB Address Boundary space, and the top is one less than a 4-KB Address Boundary space.		
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8.2.18 Register Offset 01Dh -- I/O Limit Register

Bit(s)	Description	CFG	Default
3:0	I/O Limit Address Capability Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are <i>reserved</i> . The value returned in this field is derived from the I/O Base register <i>I/O Base Address Capability</i> field.	RO	0h
7:4	I/O Limit Determines the I/O Space range forwarded from the primary bus to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the Bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary side of the Bridge, the <i>I/O Limit</i> field is programmed to a value smaller than the I/O Base register <i>I/O Base</i> field. In this case, the Bridge does not forward I/O transactions from the primary bus to the secondary bus; however, the Bridge does forward all I/O transactions from the secondary bus to the primary bus.	RW	0h

8.2.19 Register Offset 01Eh -- Secondary Status Register

Bit(s)	Description	CFG	Default
4:0	<i>Reserved</i>		
5	Secondary 66 MHz Capable Indicates whether the Bridge's secondary bus is capable of operating at 66 MHz.	RO	0
6	<i>Reserved</i>		
7	Secondary Fast Back-to-Back Transactions Capable Indicates whether the Bridge's secondary bus is capable of decoding Fast Back-to-Back transactions when the transactions are from the same Master but to different Targets. (A bridge is required to support Fast Back-to-Back transactions from the same Master.) The Bridge does <i>not support</i> Fast Back-to-Back decoding.	RO	0
8	Secondary Master Data Parity Error Reports Data Parity error detection by the Bridge, when the bridge is the transaction Master on the secondary bus. Set when the following	RW1C	0

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	<p>three conditions are true:</p> <ul style="list-style-type: none"> • Bridge is the PCI Master of the transaction on the secondary bus • Bridge asserted PERR# (Read transaction) or detected that PERR# is asserted (Write transaction) • Bridge Control register <i>Secondary Parity Error Response Enable</i> bit is set <p>Writing 1 clears this bit.</p>		
10:9	<p>Secondary DEVSEL Timing Encodes the secondary bus DEVSEL# timing. The encoding must indicate the slowest response time that the Bridge uses to assert DEVSEL# on its secondary bus when responding as a Target to a transaction other than a Configuration Read or Write.</p> <p>01b = Indicates medium DEVSEL# timing</p> <p><i>Note: Hardwired to 01b.</i></p>	RO	01b
11	<p>Secondary Signaled Target Abort Reports Target Abort termination signaling by the Bridge when the Bridge responds as the transaction Target on its secondary bus.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
12	<p>Secondary Received Target Abort Reports Target Abort termination detection by the Bridge when the bridge is the transaction Master on its secondary bus.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
13	<p>Secondary Received Master Abort Reports Master Abort termination detection by the Bridge when the bridge is the transaction Master on its secondary bus. Also set for a PCI Express-to-PCI Configuration transaction with an extended address not equal to 0.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
14	<p>Secondary Received System Error Reports SERR# assertion detection on the Bridge's secondary bus.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
15	<p>Secondary Detected Parity Error Reports Address or Data Parity error detection by the Bridge on its secondary bus. Set when any of the following three conditions are true:</p> <ul style="list-style-type: none"> • Bridge detects an Address Parity error as a potential Target • Bridge detects a Data Parity error when the Bridge is a Write transaction Target • Bridge detects a Data Parity error when the Bridge is a Read transaction Master <p>Set irrespective of the Bridge Control register <i>Secondary</i></p>	RW1C	0

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	<i>Parity Error Response Enable</i> bit state. Writing 1 clears this bit.		
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8.2.20 Register Offset 020h -- Memory Base Register

Bit(s)	Description	CFG	Default
3:0	Reserved <i>Note: Hardwired to 0h.</i>		00h
15:4	Memory Base Determines the starting address at which Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the Bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are 0_0000h. The bottom of the defined Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.	RW	

8.2.21 Register Offset 022h -- Memory Limit Register

Bit(s)	Description	CFG	Default
3:0	Reserved <i>Note: Hardwired to 0h.</i>		00h
15:4	Memory Limit Determines the Memory Space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the Bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are F_FFFFh. When there are no Memory-Mapped I/O addresses on the secondary side of the Bridge, the <i>Memory Limit</i> field must be programmed to a value smaller than the Memory Base register <i>Memory Base</i> field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the Bridge, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	

8.2.22 Register Offset 024h -- Prefetchable Memory Base Register

Bit(s)	Description	CFG	Default
3:0	Prefetchable Base Address Capability Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address	RO	00h

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	All other encodings are <i>reserved</i> .		
15:4	<p>Prefetchable Memory Base Determines the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the Bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are 0_0000h.</p> <p>The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.</p>	RW	

8.2.23 Register Offset 026h -- Prefetchable Memory Limit Register

Bit(s)	Description	CFG	Default
3:0	<p>Prefetchable Limit Address Capability Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other encodings are <i>reserved</i>. The value returned in this field is derived from the Prefetchable Memory Base register <i>Prefetchable Base Address Capability</i> field.</p>	RO	00h
15:4	<p>Prefetchable Memory Limit Determines the Prefetchable Memory space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the Bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are F_FFFFh. When there is no prefetchable memory on the secondary side of the Bridge, the <i>Prefetchable Memory Limit</i> field must be programmed to a value smaller than the Prefetchable Memory Base register <i>Prefetchable Memory Base</i> field. When there is no Prefetchable memory, and no Memory Mapped I/O on the secondary side of the Bridge, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.</p>	RW	

8.2.24 Register Offset 028h -- Prefetchable Base Upper 32 Bits Register

Bit(s)	Description	CFG	Default
31:0	<p>Prefetchable Memory Base Upper 32 Bits When the Prefetchable Memory Base register <i>Prefetchable Base Address Capability</i> field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the <i>Prefetchable Base Address Capability</i> field indicates 64-bit addressing, this register determines the upper 32 bits of</p>	RW	00h

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	the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus.		
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8.2.25 Register Offset 02Ch -- Prefetchable Limit Upper 32 Bits Register

Bit(s)	Description	CFG	Default
31:0	<p>Prefetchable Memory Limit Upper 32 Bits When the Prefetchable Memory Limit register <i>Prefetchable Limit Address Capability</i> field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the <i>Prefetchable Limit Address Capability</i> field indicates 64-bit addressing, this register determines the upper 32 bits of the Prefetchable Memory range forwarded from the primary bus to the secondary bus.</p>	RW	00h

8.2.26 Register Offset 030h -- I/O Base Upper 16 Bits Register

Bit(s)	Description	CFG	Default
15:0	<p>I/O Base Upper 16 Bits When the I/O Base register <i>I/O Base Address Capability</i> field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the <i>I/O Base Address Capability</i> field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus.</p>	RW	

8.2.27 Register Offset 030h -- I/O Limit Upper 16 Bits Register

Bit(s)	Description	CFG	Default
15:0	<p>I/O Limit Upper 16 Bits When the I/O Limit register <i>I/O Limit Address Capability</i> field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the <i>I/O Limit Address Capability</i> field indicates 32-bit addressing, this register determines the upper 16 bits of the I/O range forwarded from the primary bus to the secondary bus.</p>	RW	

8.2.28 Register Offset 034h -- Capabilities Pointer Register

Bit(s)	Description	CFG	Default
7:0	<p>PCI Capabilities Pointer Provides the offset location of the first New Capabilities register</p>	RO	40h

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31:8	<i>Reserved</i>		
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8.2.29 Register Offset 038h -- Expansion ROM base address Register

Bit(s)	Description	CFG	Default
0	<p>Expansion ROM base address</p> <p>Address Decode Enable.</p> <p>1= indicates the device accepts accesses to the expansion ROM address.</p> <p>0= indicates the device does not accept accesses to expansion ROM space.</p> <p>Should be set to 0 if no Expansion ROM.</p>	RW	0
10:1	Reserved		0
31:11	Expansion ROM Base Address (upper 21 bits)	RW	0

8.2.30 Register Offset 03Ch -- Interrupt Line Register

Bit(s)	Description	CFG	Default
7:0	<p>PCI Interrupt Line</p> <p>Indicates to which System Interrupt Controller input the Bridge Interrupt is connected. Device drivers and operating systems use this field.</p>	RW	40h

8.2.31 Register Offset 03Dh -- Interrupt Pin Register

Bit(s)	Description	CFG	Default
7:0	<p>PCI Interrupt Pin</p> <p>Identifies the Conventional PCI Interrupt message(s) used by the Bridge. Valid values are 1, 2, 3, and 4, which map to Conventional PCI Interrupt messages for INTA#, INTB#, INTC#, and INTD#, respectively.</p> <p>0h = Indicates that the Bridge does not use Conventional PCI Interrupt messages</p>	RO	1h

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8.2.32 Register Offset 03Eh -- Bridge Control Register

Bit(s)	Description	CFG	Default
0	<p>Secondary Parity Error Response Enable Controls the Bridge's response to Address and Data Parity errors on the secondary bus (PCI). 0 = must ignore detected Parity errors and continue standard operation. A bridge must generate parity, regardless of whether Parity error reporting is disabled. Also, the Bridge must always forward Posted. Write data with poisoning, from PCI-to-PCI Express on a PCI Data Parity error, regardless of this bit's setting. 1 = must take its standard action when a Parity error is detected.</p>	RW	0
1	<p>Secondary SERR# Enable Controls forwarding of secondary bus (PCI) SERR# assertions to the primary bus (PCI Express). The Bridge transmits an ERR_FATAL message on the primary bus when all of the following are true: <ul style="list-style-type: none"> • SERR# is asserted on the secondary bus • This bit is set • PCI Command register <i>SERR# Enable</i> bit is set or PCI Express Device Control register <i>Fatal Error Reporting Enable</i> or <i>Non-Fatal Error Reporting Enable</i> bit is set </p>	RW	0
2	<p>ISA Enable Modifies the Bridge's response to ISA I/O addresses that are enabled by the I/O Base and I/O Limit registers and located in the first 64 KB of the PCI I/O Address space. 1 = Bridge blocks forwarding from the primary bus to the secondary bus of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.</p>	RW	0
3	<p>VGA Enable Modifies the Bridge's response to VGA-compatible addresses. When set to 1, the Bridge positively decodes and forwards the following accesses on the primary bus to the secondary bus (and, conversely, blocks the forwarding of these addresses from the secondary bus to the primary bus): <ul style="list-style-type: none"> • Memory accesses within the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is within the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When set to 1, VGA address forwarding is independent of the: <ul style="list-style-type: none"> • Bit 2 (<i>ISA Enable</i>) setting • Memory and I/O Address ranges defined by the I/O Base, I/O Limit, Memory Base, Memory Limit, Prefetchable Memory Base, and Prefetchable Memory Limit registers </p>	RW	0

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	<p>forwarding is qualified by the PCI Command register <i>I/O Access Enable</i> and <i>Memory Space Enable</i> bits.</p> <p>0 = Does not forward VGA-compatible Memory and I/O addresses from the primary bus to the secondary bus (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges</p> <p>1 = Forwards VGA-compatible Memory and I/O addresses (addresses defined above) from the primary bus to the secondary bus (when the <i>I/O Access Enable</i> and <i>Memory Space Enable</i> bits are set), independent of the I/O and Memory Address ranges and <i>ISA Enable</i> bit</p>		
4	<p>VGA 16-Bit Decode Enables the Bridge to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (<i>VGA Enable</i>) is also set to 1, enabling VGA I/O decoding and bridge forwarding. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary bus to the secondary bus, when the <i>VGA Enable</i> bit is set to 1.</p> <p>0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses</p>		0
5	<p>Master Abort Mode Controls the Bridge's behavior when it receives a Master Abort termination on the PCI Bus or an Unsupported Request on the PCI Express interface.</p> <p>0 = Do not report Master Aborts</p> <ul style="list-style-type: none"> • When a PCI Express UR is received: <ul style="list-style-type: none"> – Return FFFF_FFFFh to the PCI Bus for Reads – Complete Non-Posted Write normally on the PCI Bus (assert <i>TRDY#</i>) and discard the Write data – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: <ul style="list-style-type: none"> – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI <p>1 = Report Master Aborts</p> <ul style="list-style-type: none"> • When a PCI Express UR is received: <ul style="list-style-type: none"> – Complete Reads and Non-Posted Writes with a PCI Target Abort – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: <ul style="list-style-type: none"> – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI – Transmit <i>ERR_NONFATAL</i> message for Posted Writes 	RW	0
6	<p>Secondary Bus Reset 1 = Forces <i>PCIRSTOUT_N#</i> to be asserted on the secondary bus. Additionally, the Bridge secondary bus, and buffers between the two buses (primary and secondary), must be</p>	RW	0

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	<p>initialized to their default state.</p> <p>The primary bus and Configuration Space registers must not be affected by setting this bit. Because PCIRSTOUT_N# is asserted while this bit is set, software must observe proper PCI Reset timing requirements.</p>		
7	<p>Fast Back-to-Back Enable <i>Not supported</i></p> <p>Controls the Bridge's ability to generate Fast Back-to-Back transactions to various secondary bus devices.</p>	RO	0
8	<p>Primary Discard Timer</p> <p>In Forward Bridge mode, this bit does not apply and is forced to 0.</p>	RO	0
9	<p>Secondary Discard Timer</p> <p>Selects the number of PCI clocks that the Bridge waits for a Master on the secondary bus to repeat a Delayed Transaction request. The Counter starts after the Completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the Bridge downstream queue (<i>that is</i>, all ordering requirements are satisfied and the Bridge is ready to complete the Delayed Transaction with the originating Master on the secondary bus).</p> <p>When the originating Master does not repeat the transaction before the Counter expires, the Bridge deletes the Delayed Transaction from its queue and sets the <i>Discard Timer Status</i> bit.</p> <p>0 = Secondary Discard Timer counts 2¹⁵ PCI clock periods 1 = Secondary Discard Timer counts 2¹⁰ PCI clock periods</p>	RW	0
10	<p>Discard Timer Status</p> <p>Set to 1 when the <i>Secondary Discard Timer</i> expires and a Delayed Completion is discarded from a queue within the Bridge.</p> <p>Writing 1 clears this bit.</p>	RW1C	0
11	<p>Discard Timer SERR# Enable</p> <p>When set to 1, enables the Bridge to generate an ERR_NONFATAL message on the primary bus when the <i>Secondary Discard Timer</i> expires and a Delayed Transaction is discarded from a queue within the Bridge.</p> <p>0 = Does not generate ERR_NONFATAL message on the primary bus as a result of the <i>Secondary Discard Timer</i> expiration</p> <p>1 = Generates ERR_NONFATAL message on the primary bus when the <i>Secondary Discard Timer</i> expires and a Delayed Transaction is discarded from a queue within the Bridge</p>	RW	0
15:12	Reserved		0

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8.3 MSI Capability Structure

31:24	23:16	15:8	7:0	Byte Offset
Message Control		Next Pointer	Cap ID	050h
Message Address				054h
Message Upper Address				058h
			Message Data	05Ch

8.3.1 Register Offset 050h -- MSI Capability ID Register

Bit(s)	Description	CFG	Default
7:0	MSI Capability ID Specifies the Message Signaled Interrupt (MSI) Capability ID.	RO	05h

8.3.2 Register Offset 051h -- MSI Next Pointer Register

Bit(s)	Description	CFG	Default
7:0	MSI Next Capability Pointer Points to the first location of the next item in the New Capabilities Linked List (offset 78h, PCI Express Capability structure).	RO	78h

8.3.3 Register Offset 052h -- MSI Control Register

Bit(s)	Description	CFG	Default
0	MSI Enable 1 = Enables the Bridge to use MSI to request service. Virtual interrupt support for internal interrupt sources are disabled.	RW	0h
3:1	Multiple Message Capable System software reads this field, to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four). 000b = 1 message requested 001b = 2 messages requested 010b = 4 messages requested 011b = 8 messages requested 100b = 16 messages requested 101b = 32 messages requested 110b, 111b = <i>Reserved</i>	RO	000b
6:4	Multiple Message Enable System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two.	RW	000b

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	000b = 1 message allocated 001b = 2 messages allocated 010b = 4 messages allocated 011b = 8 messages allocated 100b = 16 messages allocated 101b = 32 messages allocated 110b, 111b = <i>Reserved</i>		
7	MSI 64-Bit Address Capable 1 = Bridge is capable of generating a 64-bit Message address	RO	0
8	Per Vector Masking Capable <i>Not supported</i> Forced to 0.	RO	0
15:9	<i>Reserved</i>		

8.3.4 Register Offset 054h -- MSI Address Register

Bit(s)	Description	CFG	Default
1:0	<i>Reserved</i>	RO	0h
31:2	MSI Address When the MSI Control register <i>MSI Enable</i> bit is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits [1:0] are driven to zero (00b) during the Address phase. <i>Note: Refer to register offset 58h for MSI Upper Address.</i>	RW	0h

8.3.5 Register Offset 058h -- MSI Upper Address Register

Bit(s)	Description	CFG	Default
31:0	MSI Upper Address Valid/used only when the Bridge supports a 64-bit Message address (MSI Control register <i>MSI 64-Bit Address Capable</i> bit is set to 1). When the MSI Control register <i>MSI Enable</i> bit is set, the register contents specify the upper 32 bits of a 64-bit message. When the register contents are zero (0h), the Bridge uses the 32-bit address specified by the MSI Address register. <i>Note: Refer to register offset 54h for MSI Address.</i>	RW	0h

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8.3.6 Register Offset 05Ch -- MSI Data Register

Bit(s)	Description	CFG	Default
15:0	MSI Data When the MSI Control register <i>MSI Enable</i> bit is set, the Message data is driven onto the lower word of the AD Bus (AD[15:0]) of the Memory Write Transaction Data phase. The upper word (AD[31:16]) is always cleared to 0h.	RW	0h
31:16	<i>Reserved</i>		

8.4 MSI-X Capability Structure

31:24	23:16	15:8	7:3	2:0	Byte Offset
Message Control		Next Pointer	Capability ID		068h
Table Offset				table BIR	06Ch
PBA Offset				PBA BIR	070h

8.4.1 Register Offset 068h -- MSI-X Capability ID Register

Bit(s)	Description	CFG	Default
7:0	MSI-X Capability ID Specifies the MSI-X Capability ID.	RO	11h

8.4.2 Register Offset 069h -- MSI-X Next Pointer Register

Bit(s)	Description	CFG	Default
7:0	MSI-X Next Capability Pointer Points to the first location of the next item in the New Capabilities Linked List (offset 78h, PCI Express Capability structure).	RO	78h

8.4.3 Register Offset 06Ah -- MSI-X Control Register

Bit(s)	Description	CFG	Default
10:0	Table Size System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of “0000000011” indicates a table size of 4.	RO	01h

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	This field is read only.		
13:11	Reserved	RO	000b
14	<p>Function Mask If 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not.</p> <p>Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits. This bit's state after reset is 0 (unmasked).</p> <p>This bit is read/write.</p>	RW	0b
15	<p>MSI-X Enable If 1 and the MSI Enable bit in the MSI Message Control register is 0, the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin.</p> <p>System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a function's service request.</p> <p>If 0, the function is prohibited from using MSI-X to request service.</p> <p>This bit's state after reset is 0 (MSI-X is disabled). This bit is read/write.</p>	RW	0

8.4.4 Register Offset 06Ch -- MSI-X Table Offset Register

Bit(s)	Description	CFG	Default
2:0	<p>Table BIR Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into Memory Space.</p> <p>BIR Value Base Address register 0 = 10h 1 = 14h 2 = 18h 3 = 1Ch 4 = 20h 5 = 24h 6 Reserved 7 Reserved</p> <p>For a 64-bit Base Address register, the Table BIR indicates the lower DWORD. With PCI-to-PCI bridges, BIR values 2 through 5 are also reserved.</p> <p>This field is read only.</p>	RO	0
31:3	<p>Table Offset Used as an offset from the address contained by one of the</p>	RO	0

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	function's Base Address registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. This field is read only.		
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8.4.5 Register Offset 070h -- MSI-X PBA Offset Register

Bit(s)	Description	CFG	Default
2:0	PBA BIR Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the MSI-X Table BIR. This field is read only.	RO	0h
31:3	PBA Offset Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. This field is read only.	RO	0h

8.5 Power Management Capability Structure

31:24	23:16	15:8	7:0	Byte Offset
Capabilities Register		Next Cap PTR	Cap ID	078h
Data	PM Control/Status Bridge Extensions	Power Management Status & Control		07Ch

8.5.1 Register Offset 078h -- Power Management Capability ID Register

Bit(s)	Description	CFG	Default
7:0	Capability ID This field is read only.	RO	01h
15:8	Next Capability Pointer This field is read only.	RO	80h

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8.5.2 Register Offset 07Ah -- Power Management Capabilities Register

Bit(s)	Description	CFG	Default
2:0	Capability Version	RO	011b
3	PME Clock Does not apply to PCI Express and must be hardwired to 0b.	RO	0
10:4	<i>Reserved</i>		
15:11	PME Support For a device Function, this 5-bit field indicates the power states in which the Function may generate a PME.	RO	00000b

8.5.3 Register Offset 07Ch -- Power Management Status & Control Register

Bit(s)	Description	CFG	Default
1:0	Power State The 2-bit field is used to determine the current power state of a function and to set the function into a new power state. The definition of the field value is given below: 00b – D0 01b – D1 10b – D2 11b – D3hot	RW	00b
7:2	<i>Reserved</i>	RO	00b
8	PME Enable Control PM_PME Message Generation 0 = Disabled 1 = Enabled	RW	0b
12:9	PM Select Data Select	RW	0000b
14:13	PM Data Scale Data Scale	RW	00b
15	PME Status	RW1C	0b
23:16	<i>Reserved</i>		
31:24	PM Data	RW	00h

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8.6 PCI Express Capability Structure

31:24	23:16	15:8	7:0	Byte Offset
Capabilities Register		Next Cap PTR	Capability ID	080h
Device capabilities				084h
Device Status		Device control		088h
Link capabilities				08Ch
Link Status		Link control		090h
Slot capabilities				094h
Slot Status		Slot Control		098h
Root Control				09Ch
Root Status				0A0h
Device capabilities 2				0A4h
Device Status 2		Device control 2		0A8h
Link capabilities 2				0ACH
Link Status 2		Link control 2		0B0h

8.6.1 Register Offset 080h -- PCI Express Capability ID Register

Bit(s)	Description	CFG	Default
7:0	PCI Express Capability ID Specifies the PCI Express Capability ID.	RO	10h

8.6.2 Register Offset 081h -- PCI Express Next Cap PTR Register

Bit(s)	Description	CFG	Default
7:0	PCI Express Next Capability Pointer 0h = Last capability in the New Capabilities Linked List	RO	00h

8.6.3 Register Offset 082h -- PCI Express Capabilities Register

Bit(s)	Description	CFG	Default
3:0	Capability Version Indicates the PCI Express Capability structure Version Number.	RO	1h
7:4	Device/Port Type Indicates the type of PCI Express logical device. 0000b = PCI Express Endpoint Device 0001b = Conventional PCI Express Endpoint Device 0100b = Root Port of PCI Express Root Complex 0101b = Upstream Port of PCI Express Switch	RO	0111b

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	0110b = Downstream Port of PCI Express Switch 0111b = PCI Express-to-PCI/PCI-X Bridge 1000b = PCI/PCI-X-to-PCI Express Bridge All other encodings are <i>reserved</i> .		
8	Slot Implemented 1 = Indicates that the PCI Express link associated with this port is connected to a slot	RO	0
13:9	Interrupt Message Number When this function is allocated more than one MSI number, this field must contain the offset between the Base Message data and MSI message generated when the Slot Status or Root Status register bits of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the Bridge changes.	RO	0h
15:14	<i>Reserved</i>		

8.6.4 Register Offset 084h -- PCI Express Device Capabilities Register

Bit(s)	Description	CFG	Default
7:0	Maximum Payload Size Supported Indicates the Maximum Payload Size that the Bridge supports for TLPs. 000b = 128 bytes All other encodings are <i>reserved</i> . <i>Note: Because the Bridge supports a Maximum Payload Size of only 128 bytes, this field is hardwired to 000b.</i>	RO	000b
4:3	Phantom Functions Supported <i>Not supported</i> Hardwired to 00b. Indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called <i>Phantom Functions</i>) with the Tag identifier.	RO	00b
5	Extended Tag Field Supported Indicates the maximum supported <i>Tag</i> field size 0 = 5-bit <i>Tag</i> field is supported 1 = 8-bit <i>Tag</i> field is supported <i>Note: 8-bit Tag field support must be enabled by the corresponding</i> <i>Control field in the PCI Express Device Control register.</i>	RO	0
8:6	Endpoint L0s Acceptable Latency Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L0s to L0 Link PM	RO	000b

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	<p>state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Link PM state Acceptable Latency number to compare against the L0s Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L0s Link PM state entry is used with no performance loss.</p> <p>000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs</p>		
11:9	<p>Endpoint L1 Acceptable Latency Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L1 to L0 Link PM state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Link PM state Acceptable Latency number to compare against the L1 Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L1 Link PM state entry is used with performance loss.</p> <p>000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs</p>	RO	000b
12	<i>Reserved</i>		
13	<i>Reserved</i>		
14	<i>Reserved</i>		
15	<p>PCI Express specification compliance This variable should be set to 1. <i>Value 0 is used for backwards-compatibility with PCIe Specification 1.0a.</i></p>	RO	1
17:16	<i>Reserved</i>		
25:18	<p>Captured Slot Power Limit Value Specifies the upper limit on power supplied by slot in combination with the <i>Slot Power Limit Scale</i> value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the <i>Slot Power Limit Scale</i> field. Value is set by the Set Slot Power Limit message.</p>	RO	0h

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27:26	Captured Slot Power Limit Scale Specifies the scale used for the <i>Slot Power Limit Value</i> . Value is set by the Set Slot Power Limit message. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	00b
31:28	<i>Reserved</i>		

8.6.5 Register Offset 088h -- PCI Express Device Control Register

Bit(s)	Description	CFG	Default
0	Correctable Error Reporting Enable Does not apply to Reverse Bridge mode.	RW	0
1	Non-Fatal Error Reporting Enable Does not apply to Reverse Bridge mode.	RW	0
2	Fatal Error Reporting Enable Does not apply to Reverse Bridge mode.	RW	0
3	Unsupported Request Reporting Enable Does not apply to Reverse Bridge mode.	RW	0
4	Enable Relaxed Ordering If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Default value of this bit is 1	RW	1
7:5	Maximum Payload Size Sets the maximum TLP Payload Size for the Bridge. As a Receiver, the Bridge must handle TLPs as large as the set value; as Transmitter, the Bridge must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the Device Capability register <i>Maximum Payload Size Supported</i> field. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = <i>Reserved</i>	RW	000b
8	Extended Tag Field Enable 0 = Bridge is restricted to a 5-bit <i>Tag</i> field 1 = Enables Bridge to use an 8-bit <i>Tag</i> field as a Requester Forced to 0 when the Device Capability register <i>Extended Tag Field Supported</i> bit is cleared.	RW	0
9	Phantom Function Enable When set, this bit enables a device to use an 8-bit <i>Tag</i> field as a requester. If the bit is cleared, the device is restricted to a 5-bit	RW	0

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	<p>Tag field.</p> <p>Default value of this field is 0.</p>		
10	<p>Auxiliary (AUX) Power PM Enable When set, this bit enables a device to draw AUX power independent of PME AUX power.</p> <p>Default value of this field is 0.</p>	RW	0
11	<p>Enable No Snoop If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiated that do not require hardware enforced cache coherency.</p> <p>Default value of this bit is 1.</p>	RW	1
14:12	<p>Maximum Read Request Size The value specified in this register is the upper boundary of the PCI Control register <i>Programmed Prefetch Size</i> field if the Device-Specific Control register <i>Blind Prefetch Enable</i> bit is set. Sets the Maximum Read Request Size for the Bridge as a Requester. The Bridge must not generate Read requests with a size that exceeds the set value. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = <i>Reserved</i></p>	RW	010b
15	<p>Bridge Configuration Retry Enable 0 = Bridge does not generate Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions 1 = Bridge generates Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions</p>	RW	0

8.6.6 Register Offset 08Ah -- PCI Express Device Status Register

Bit(s)	Description	CFG	Default
0	<p>Correctable Error Detected Does not apply to Reverse Bridge mode.</p>	RW1C	0
1	<p>Non-Fatal Error Detected Does not apply to Reverse Bridge mode.</p>	RW1C	0
2	<p>Fatal Error Detected Does not apply to Reverse Bridge mode.</p>	RW1C	0
3	<p>Unsupported Request Detected Does not apply to Reverse Bridge mode.</p>	RW1C	0

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4	AUX Power Detected Devices that require AUX power report this bit as set when the Bridge detects AUX power.	RO	0
5	Transactions Pending	RO	1
15:6	<i>Reserved</i>		

8.6.7 Register Offset 08Ch -- PCI Express Link Capabilities Register

Bit(s)	Description	CFG	Default
3:0	Maximum Link Speed Indicates the maximum link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are <i>reserved</i> .	RO	0001b
9:4	Maximum Link Width Indicates the maximum width of the given PCI Express link. By default, the Bridge has a x1 link; therefore, this field is hardwired to 00_0001b. All other encodings are <i>not supported</i> .	RO	00_0001b
11:10	Active State Power Management (ASPM) Support Indicates the level of ASPM supported on the given PCI Express link. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported 00b, 10b = <i>Reserved</i>	RO	01b
14:12	L0s Exit Latency Indicates the L0s Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L0s to L0 Link PM state. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μ s 101b = 1 μ s to less than 2 μ s 110b = 2 to 4 μ s 111b = More than 4 μ s	RO	101b
17:15	L1 Exit Latency Indicates the L1 Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L1 to L0 Link PM state. 000b = Less than 1 μ s 001b = 1 μ s to less than 2 μ s 010b = 2 μ s to less than 4 μ s 011b = 4 μ s to less than 8 μ s 100b = 8 μ s to less than 16 μ s 101b = 16 μ s to less than 32 μ s	RO	001b

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	110b = 32 to 64 μ s 111b = More than 64 μ s		
23:18	<i>Reserved</i>		
31:24	Port Number Indicates the PCI Express Port Number for the given PCI Express link.	RO	1h

8.6.8 Register Offset 090h -- PCI Express Link Control Register

Bit(s)	Description	CFG	Default
1:0	Active State Power Management (ASPM) Control Controls the level of ASPM supported on the given PCI Express link. 00b = Disabled 01b = L0s Entry Enable 10b = L1 Entry Enable 11b = L0s and L1 Entry Enable <i>Note: "L0s Entry Enabled" indicates the Transmitter entering the L0s Link PM state. The Receiver must be capable of entering L0s even when the field is disabled(00b).</i>	RW	00b
2	<i>Reserved</i>		
3	Read Completion Boundary (RCB) Control 0 = Read Completion boundary is 64 bytes 1 = Read Completion boundary is 128 bytes	RO	0
4	Link Disable Disables the link when set to 1. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RW	0
5	Retrain Link 1 = Initiates link retraining Always returns 0 when read.	RW	0
6	Common Clock Configuration 0 = Indicates that the Bridge and the component at the opposite end of the link are operating with asynchronous Reference Clock. Components utilize this common clock configuration information to report the correct L0s and L1 Link PM state Exit Latencies. 1 = Indicates that the Bridge and the component at the opposite end of the link are operating with a distributed common Reference Clock.	RW	0
7	Extended Sync 1 = Forces extended transmission of FTS Ordered-Sets in FTS and extra TS2 at exit from the L1 Link PM state prior to entering the L0 Link PM state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters the L0 Link PM state and	RW	0

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	resumes communication.		
15:8	<i>Reserved</i>		

8.6.9 Register Offset 092h -- PCI Express Link Status Register

Bit(s)	Description	CFG	Default
3:0	Link Speed Indicates the negotiated link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are <i>reserved</i> .	RO	0001b
9:4	Negotiated Link Width Indicates the negotiated width of the given PCI Express link. By default, the Bridge has a x1 link	RO	00_0001b
10	Link Training Error Indicates that a Link Training error occurred. Cleared by hardware upon successful training of the link to the L0 Link PM state.	RO	0
11	Link Training Indicates that link training is in progress; hardware clears this bit after link training is complete	RO	0
12	Slot Clock Configuration Indicates that the Bridge uses the same physical Reference Clock that the platform provides on the connector. When the Bridge uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.		
15:13	<i>Reserved</i>		

8.6.10 Register Offset 094h -- PCI Express Slot Capabilities Register

Bit(s)	Description	CFG	Default
0	Attention Button Present When set to 1b, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.	RO	0
1	Power Controller Present When set to 1b, this bit indicates that a software programmable Power Controller is implemented for this slot.	RO	0
2	MRL Sensor Present When set to 1b, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.	RO	0

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3	Attention Indicator Present When set to 1b, this bit indicates that an Attention Indicator is electrically controlled by the chassis.	RO	0
4	Power Indicator Present When set to 1b, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.	RO	0
5	Hot Plug Surprise When set to 1b, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification.	RO	0
6	Hot Plug Capable When set to 1b, this bit indicates that this slot is capable of supporting hot-plug operations.	RO	0
14:7	Slot Power Limit Value In combination with the <i>Slot Power Limit Scale</i> value, specifies the upper limit on power supplied by the slot. The Power Limit (in Watts) is calculated by multiplying the value in this field by the value in the <i>Slot Power Limit Scale</i> field. Writes to this register cause the Bridge to transmit the Set Slot Power Limit message downstream.	RO	0
16:15	Slot Power Limit Scale Specifies the scale used for the <i>Slot Power Limit Value</i> . Writes to this register cause the Bridge to transmit the Set Slot Power Limit message downstream. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	0
18:17	Reserved	RO	0
31:19	Physical Slot Number This hardware initialized field indicates the physical slot number attached to this Port.	RO	0

8.6.11 Register Offset 098h -- PCI Express Slot Control Register

Bit(s)	Description	CFG	Default
0	Attention Button Pressed Enable When set to 1b, this bit enables software notification on an attention button pressed event.	RW	0
1	Power Fault Detected Enable When set to 1b, this bit enables software notification on a power fault event.	RW	0
2	MRL Sensor Changed Enable When set to 1b, this bit enables software notification on a MRL	RW	0

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	sensor changed event.		
3	Presence Detect Changed Enable When set to 1b, this bit enables software notification on a presence detect changed event.	RW	0
4	Command Completed Interrupt Enable When set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller.	RW	0
5	Hot Plug Interrupt Enable When set to 1b, this bit enables generation of an interrupt on enabled hot-plug events.	RW	0
7:6	Attention Indicator Control If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off	RW	11b
9:8	Power Indicator Control If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off	RW	11b
10	Power Controller Control If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Defined encodings are: 0b Power On 1b Power Off	RW	0
15:11	<i>Reserved</i>		

8.6.12 Register Offset 09Ah -- PCI Express Slot Status Register

Bit(s)	Description	CFG	Default
0	Attention Button Pressed If an Attention Button is implemented, this bit is set when the attention button is pressed.	RW1C	0
1	Power Fault Detected If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot.	RW1C	0

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2	MRL Sensor Changed If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected.	RWIC	0
3	Presence Detect Changed This bit is set when the value reported in Presence Detect State is changed.	RWIC	0
4	Command Completed If Command Completed notification is supported, this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command.	RWIC	0
5	MRL Sensor State This register reports the status of the MRL sensor if implemented. Defined encodings are: 0b MRL Closed 1b MRL Open	RO	0
6	Presence Detect State This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Defined encodings are: 0b Slot Empty 1b Card Present in slot	RO	0
15:7	Reserved		

8.6.13 Register Offset 09Ch -- PCI Express Root Control Register

Bit(s)	Description	CFG	Default
0	System Error on Correctable Error Enable If set, this bit indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself. Default value of this field is 0.	RW	0
1	System Error on Non-Fatal Error Enable If set, this bit indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself. Default value of this field is 0.	RW	0
2	System Error on Fatal Error Enable If set, this bit indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy	RW	0

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	associated with this Root Port, or by the Root Port itself. Default value of this field is 0.		
3	PME Interrupt Enable This bit when set enables interrupt generation upon receipt of a PME Message as reflected in the PME Status register bit. Default value of this field is 0.	RW	0
4	CRS Software Visibility Enable This bit when set enables the Root Port to return Configuration Request Retry Status Completion Status to software. Default value of this field is 0.	RW	0
15:5	<i>Reserved</i>		

8.6.14 Register Offset 0A0h -- PCI Express Root Status Register

Bit(s)	Description	CFG	Default
15:0	PME requestor ID This field indicates the PCI requestor ID of the last PME requestor.	RO	0
16	PME Status This bit indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1.	RWIC	0
17	PME Pending This read-only bit indicates that another PME is pending when The PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.	RO	0
31:18	<i>Reserved</i>		

8.6.15 Register Offset 0A4h -- PCI Express Device capabilities 2 Register

Bit(s)	Description	CFG	Default
3:0	Completion Timeout Ranges Supported This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value.	RW	0000b

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	<p>This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b.</p> <p>Four time value ranges are defined: Range A: 50 μs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s</p> <p>Bits are set according to the table below to show timeout value ranges supported.</p> <p>0000b Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 μs to 50 ms. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C 1110b Ranges B, C and D 1111b Ranges A, B, C, and D</p> <p>All other values are reserved.</p>		
4	<p>Completion Timeout Disable Supported A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express.</p> <p>This mechanism is optional for Root Ports. For all other Functions this field is reserved and must be hardwired to 0b.</p>	RW	0
31:5	<i>Reserved</i>		0

8.6.16 Register Offset 0A8h -- PCI Express Device control 2 Register

Bit(s)	Description	CFG	Default
3:0	<p>Completion Timeout Value In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express.</p> <p>For all other Functions this field is reserved and must be hardwired to 0000b.</p>	RW	0000b

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	<p>A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 μs to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field.</p> <p>Defined encodings: 0000b Default range: 50 μs to 50 ms</p> <p>Values available if Range A (50 μs to 10 ms) programmability range is supported: 0001b 50 μs to 100 μs 0010b 1 ms to 10 ms</p> <p>Values available if Range B (10 ms to 250 ms) programmability range is supported: 0101b 16 ms to 55 ms 0110b 65 ms to 210 ms</p> <p>Values available if Range C (250 ms to 4 s) programmability range is supported: 1001b 260 ms to 900 ms 1010b 1 s to 3.5 s</p> <p>Values available if the Range D (4 s to 64 s) programmability range is supported: 1101b 4 s to 13 s 1110b 17 s to 64 s</p> <p>Values not defined above are reserved.</p> <p>The default value for this field is 0000b.</p>		
4	<p>Completion Timeout Disable When Set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b. Software is permitted to Set or Clear this bit at any time. When Set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests.</p> <p>If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued.</p> <p>The default value for this bit is 0b.</p>	RW	0
31:5	Reserved	RO	0

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8.6.17 Register Offset 0AAh -- PCI Express Device status 2 Register

8.6.18 Register Offset 0ACh -- PCI Express Link capabilities 2 Register

8.6.19 Register Offset 0B0h -- PCI Express Link control 2 Register

Bit(s)	Description	CFG	Default
3:0	<p>Target Link Speed For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences.</p> <p>Defined encodings are: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s Target Link Speed</p> <p>All other encodings are reserved.</p> <p>If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component unless the corresponding platform/form factor requires a different default value.</p>	RW	0000b
4	<p>Enter Compliance Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link.</p> <p>Default value of this bit following Fundamental Reset is 0b.</p>	RW	0
5	<p>Hardware Autonomous Speed Disable When Set, this bit disables hardware from changing the Link speed for device specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit.</p> <p>Default value of this bit is 0b.</p>		
6	<p>Selectable De-emphasis When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component.</p> <p>Encodings: 1b -3.5 dB 0b -6 dB</p> <p>When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.</p>	RO	0
9:7	<p>Transmit Margin This field controls the value of the non-deemphasized voltage level at the Transmitter pins.</p> <p>This field is reset to 000b on entry to the LTSSM Polling.</p>	RW	000b

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	Configuration. Encodings: 000b Normal operating range		
10	Enter Modified Compliance When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling. Compliance. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.		
11	Compliance SOS When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b.		
12	Compliance De-emphasis This bit sets the de-emphasis level in Polling. Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB		
31:13	<i>Reserved</i>		

8.6.20 Register Offset 0B2h -- PCI Express Link Status 2 Register

Bit(s)	Description	CFG	Default
0	Current De-emphasis Level When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0b.	RO	0

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8.7 SSID / SSVID Capability Structure

31:24	23:16	15:9	8	7:6	5:0	Byte Offset
reserved		Next Cap PTR			Capability ID	0C0h
SSID		SSVID				0C4h
GPIO MODE		GPIO INOUT				0C8h
			PDN		Clock Out Enable	0CCh
GPIO Pull Up		GPIO Pull Down				0D0h

8.7.1 Register Offset 0C0h -- SSID/SSVID Capability ID Register

Bit(s)	Description	CFG	Default
7:0	Capability ID Specifies the Capability ID.	RO	00h

8.7.2 Register Offset 0C1h -- SSID/SSVID Next Capability Pointer Register

Bit(s)	Description	CFG	Default
7:0	Next Capability Pointer Points to the first location of the next item in the New Capabilities Linked List	RO	00h

8.7.3 Register Offset 0C4h -- SSVID Register

Bit(s)	Description	CFG	Default
7:0	SSVID	RO	00h

8.7.4 Register Offset 0C6h -- SSID Register

Bit(s)	Description	CFG	Default
7:0	SSID	RO	00h

8.7.5 Register Offset 0C8h -- GPIO INOUT Register

Bit(s)	Description	CFG	Default
15:0	GPIO INOUT	RW	00h

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8.7.6 Register Offset 0C8h -- GPIO MODE Register

Bit(s)	Description	CFG	Default
15:0	GPIO MODE	RW	00h

8.7.7 Register Offset 0CCh -- Clock Out Enable Register

Bit(s)	Description	CFG	Default
5:0	Clock Out Enable	RW	11111b

8.7.8 Register Offset 0CDh -- PDN Register

Bit(s)	Description	CFG	Default
0	PDN	RW	0

8.7.9 Register Offset 0CEh -- PORT DECODE SELECTION Register

Bit(s)	Description	CFG	Default
0	PORT DECODE SELECTION 1 = Decode port 84; 0 = Decode port 80&90	RW	0

8.7.10 Register Offset 0CFh -- SSID SSVID Enable Register

Bit(s)	Description	CFG	Default
0	SSID SSVID Enable 1 = Indicates that the SSID SSVID can be changed.	RW	0

8.7.11 Register Offset 0D0h -- GPIO Pull Down Register

Bit(s)	Description	CFG	Default
15:0	GPIO Pull Down	RW	0h

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8.7.12 Register Offset 0D0h -- GPIO Pull Up Register

Bit(s)	Description	CFG	Default
15:0	GPIO Pull Up	RW	0h

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9. TOP MARKING SPECIFICATIONS



1st line: Nuvoton logo

2nd line: part number: NCT5868D

3rd line: tracking code 910G9AE902B006FB

910: packages made in '09, week 10

G: assembly house ID; G means GR, A means ASE, etc.

9: code version; 9 means code 009

A: IC revision; A means version A; B means version B, and C means version C

E902B006: wafer production series lot number

FA: Nuvoton internal use.

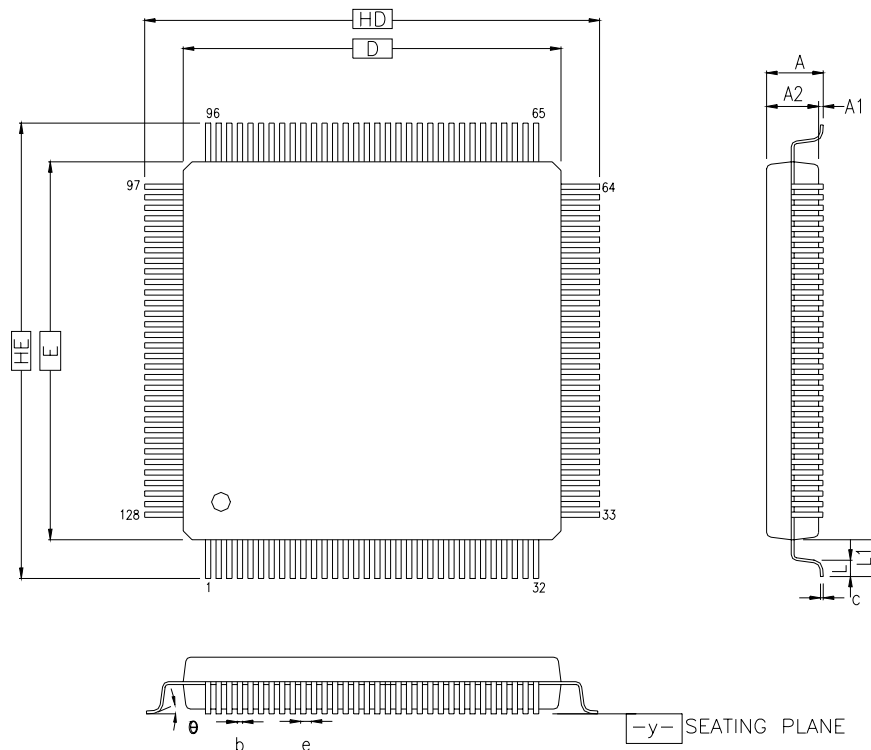
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10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT5868D	128Pin LQFP	Commercial, 0°C to +70°C

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11. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 REF			0.039 REF		
y	—	—	0.1	—	—	0.004

128-pin (LQFP)

PRELIMINARY

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	12/21/2009	N.A.	Draft version
0.2	02/23/2010	N.A	Draft version
0.21	03/16/2010	N.A	Correct pin name for pin description
0.25	05/24/2010	N.A	Add register set description
0.26	06/01/2010	62	Add Rx0CFh, bit0 for support SSID & SSVID
0.4	07/01/2010	16	Add feature description
0.41	07/06/2010	19	Add feature description

PRELIMINARY**Important Notice**

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